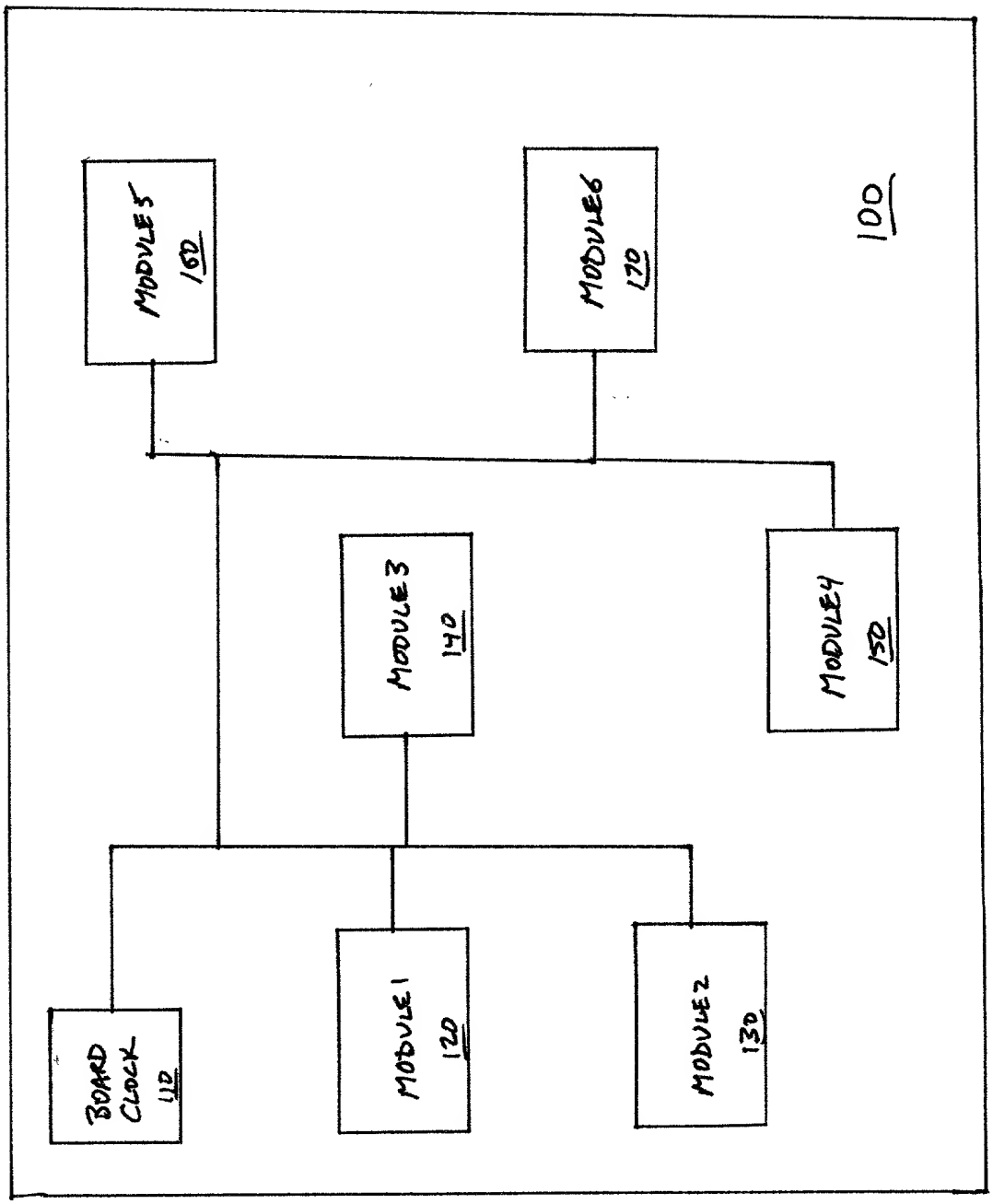
100
MODULE 5
160
MODULE 6
170
MODULE 3
140
MODULE 4
150
BOARD CLOCK
110
MODULE 1
120
MODULE 2
130

FIGURE 1

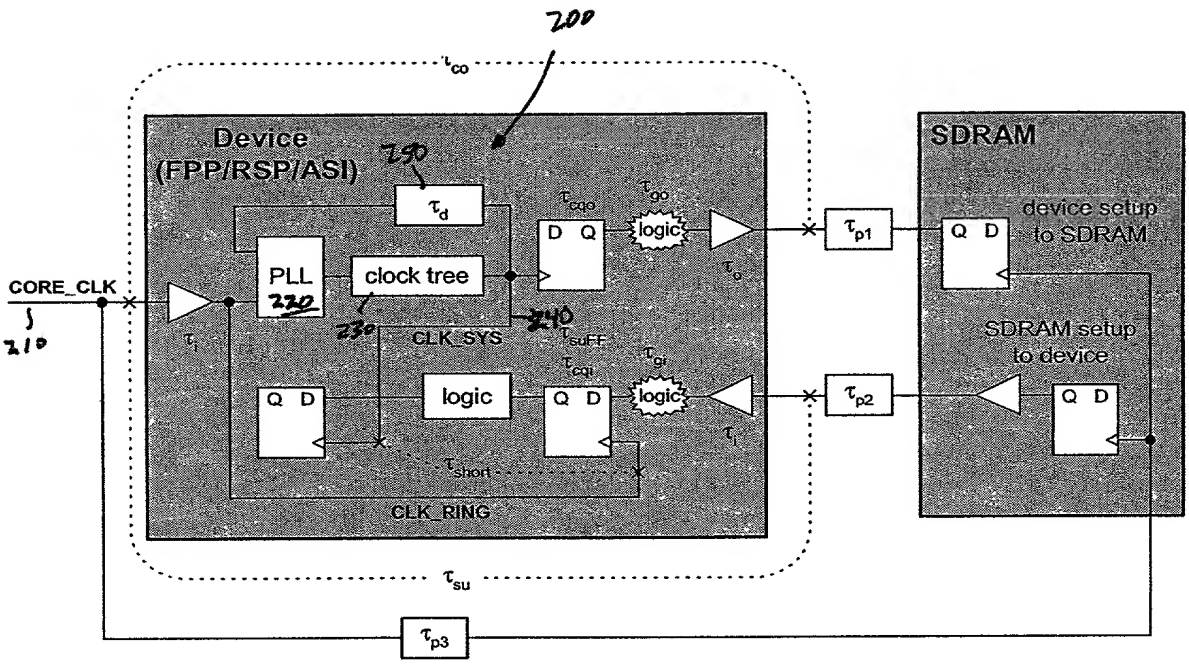
200
τ_{co}
Device
(FPP/RSP/ASI)
250
τ_d
τ_{cqo}
τ_{go}
D Q
logic
τ_o
PLL
230
clock tree
240
CORE_CLK
210
τ_i
CLK_SYS
τ_{suFF}
τ_{cqi}
τ_{gi}
Q D
logic
Q D
logic
τ_i
τ_{short}
CLK_RING
τ_{su}
τ_{p1}
τ_{p2}
τ_{p3}
SDRAM
device setup
to SDRAM
Q D
SDRAM setup
to device
Q D
Q D

FIGURE 2

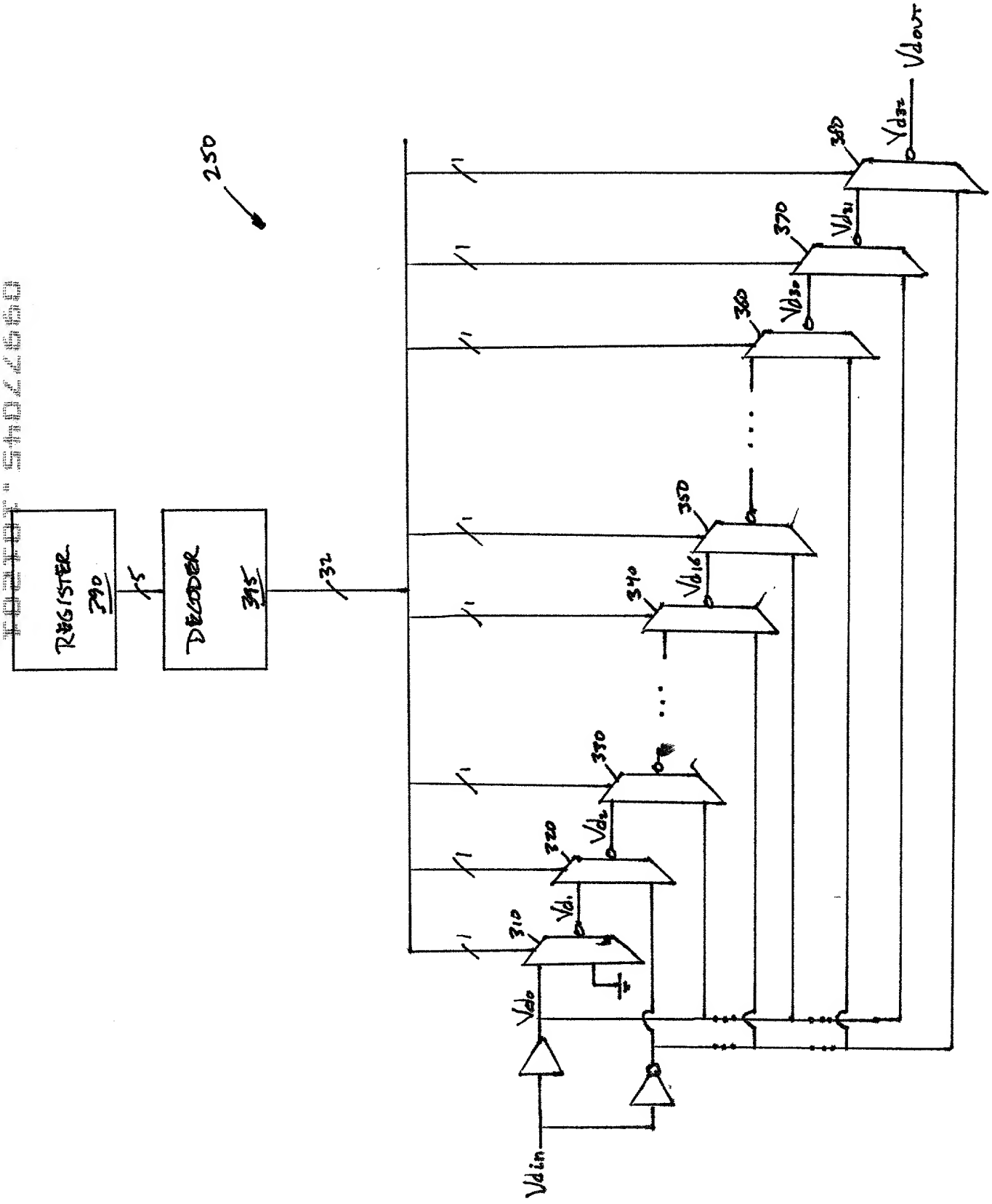
250
REGISTER
390
5
DECODER
395
32
310
320
330
340
350
360
370
380
Vd0
Vd1
Vd2
Vd16
Vd31
Vd32
Vdout
Vdin

FIGURE 3

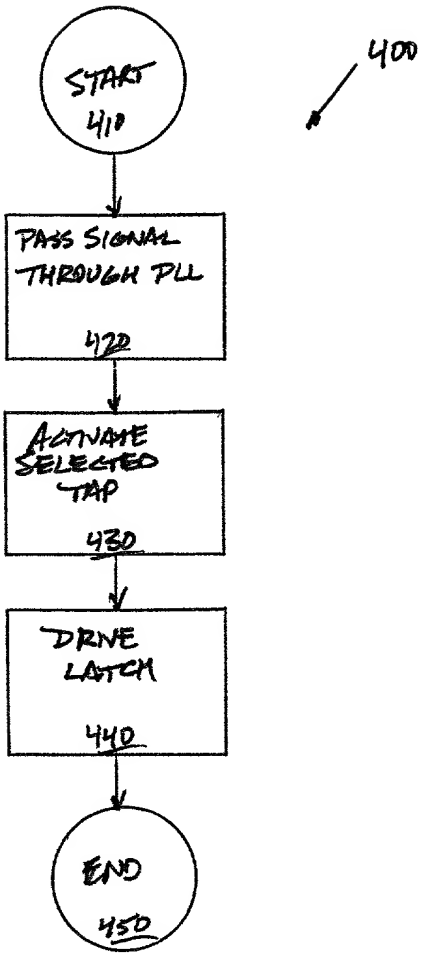
400
START
410
PASS SIGNAL THROUGH PLL
420
ACTIVATE SELECTED TAP
430
DRIVE LATCH
440
END
450

FIGURE 4